

Flynn, Thiel, et al
OPS Case 259
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Serial#08/034999
Batch#2413
Group#11108

5473616

APPROVED	O.G. FIG.	1
BY	CLASS	SUBCLASS
DRAFTSMAN	37	20.

FIG. I

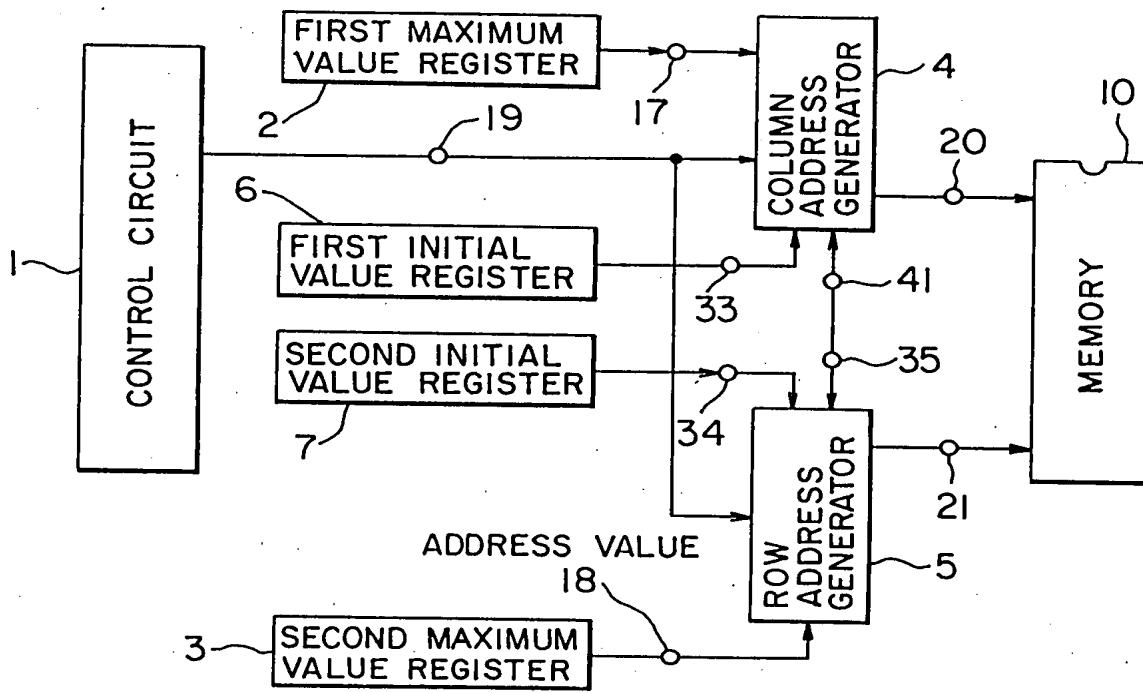


FIG. 2

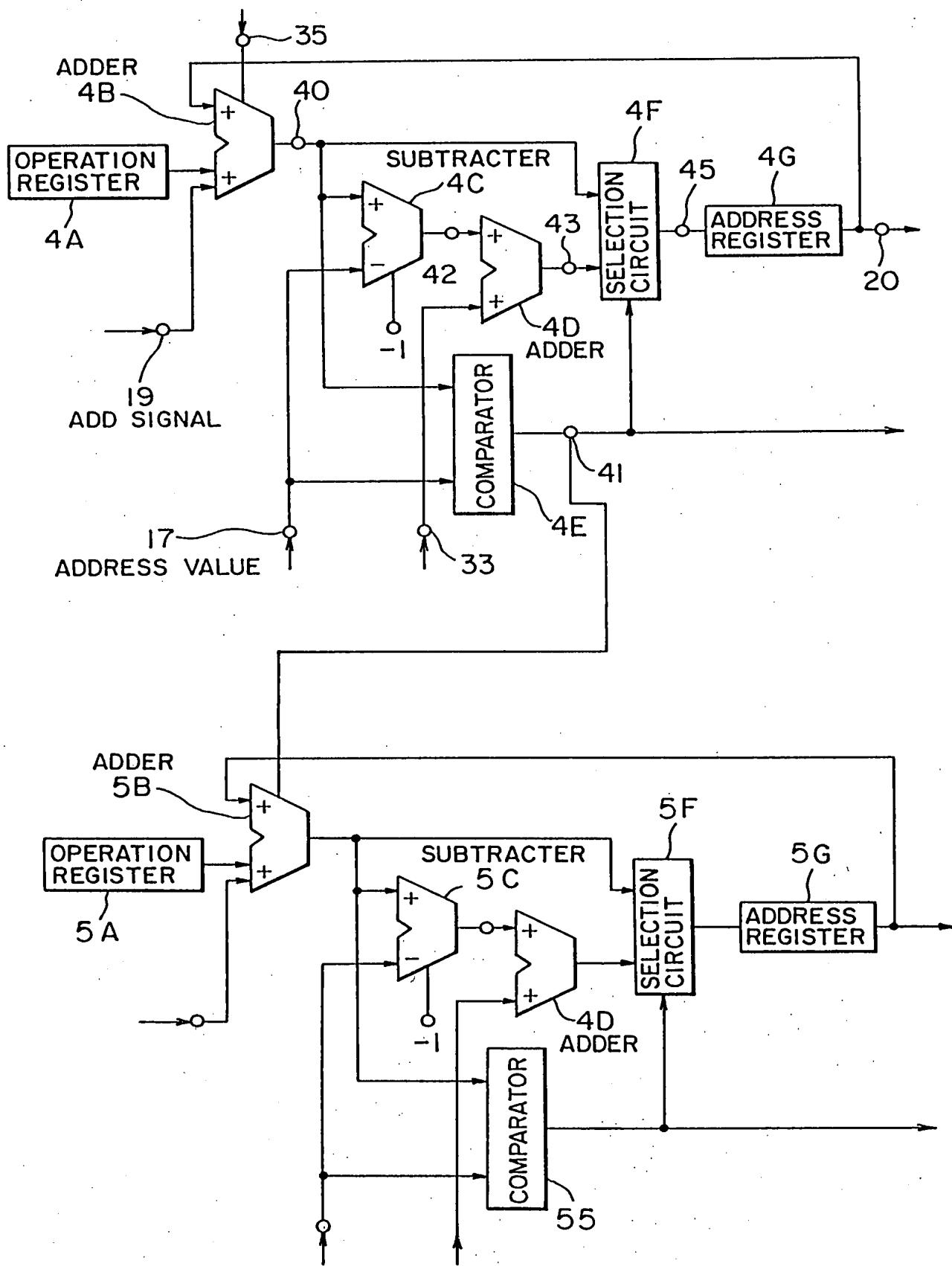


FIG. 3

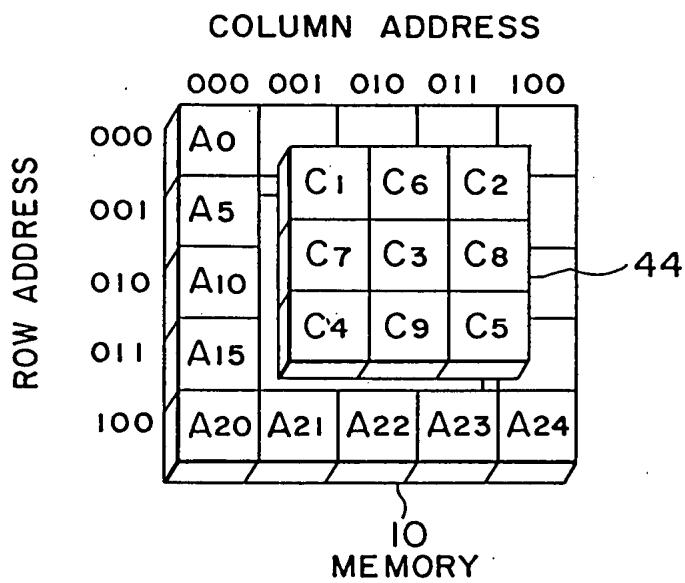
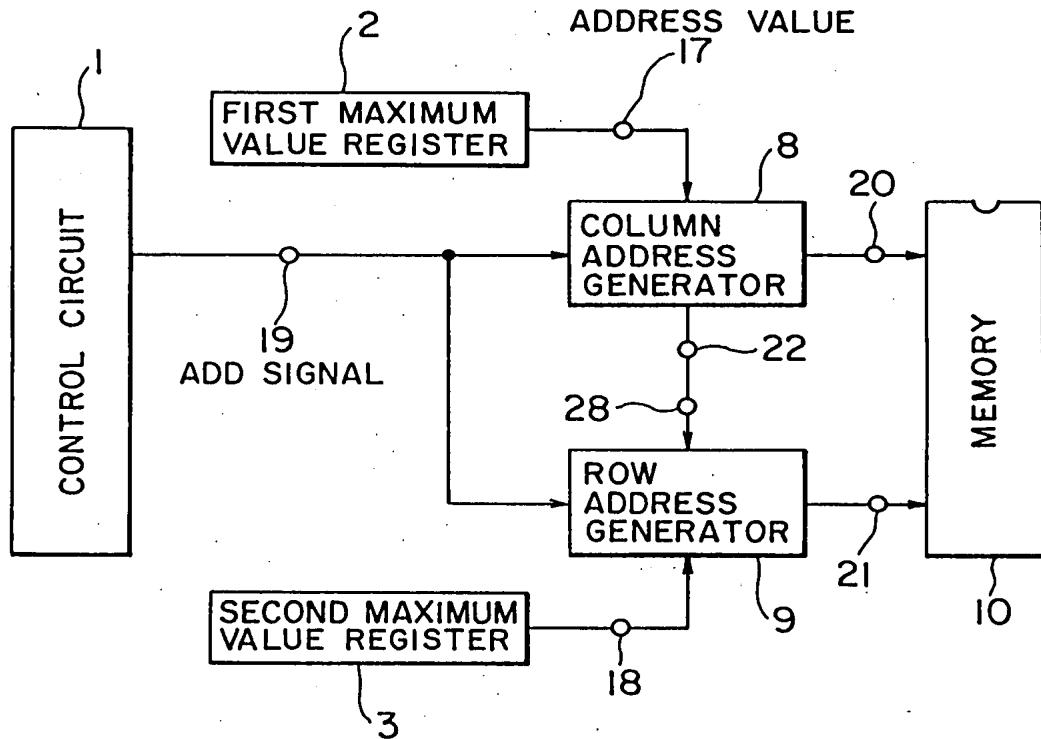


FIG. 4
PRIOR ART



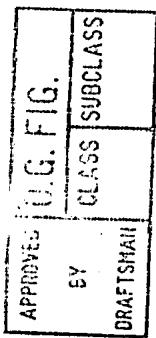


FIG. 5
PRIOR ART

The diagram illustrates a 4x4 memory grid. The vertical axis is labeled "ROW ADDRESS" and the horizontal axis is labeled "COLUMN ADDRESS". The grid contains 16 memory locations, indexed as follows:

	000	001	010	011
000	A ₀	A ₁	A ₂	A ₃
001	A ₄	A ₅	A ₆	A ₇
010	A ₈	A ₉	A ₁₀	A ₁₁
011	A ₁₂	A ₁₃	A ₁₄	A ₁₅

A bracket at the bottom right indicates the total width of the memory is 10 bits.

FIG. 6

PRIOR ART

